WHAT IS CLAIMED IS

1. An integrated circuit, comprising a shielding element.

2. The integrated circuit of claim 1, wherein the shielding element comprises a dielectric layer disposed above a low conductance semiconductor region.

3. The integrated circuit of claim 2, wherein the dielectric layer comprises gate oxide.

4. The integrated circuit of claim 3, wherein the shielding element further comprises a gate electrode layer disposed above the gate oxide layer.

5. The integrated circuit of claim 4, further comprising a charge dissipating element connecting the gate electrode layer to ground.

6. The integrated circuit of claim 5, wherein the shielding element electrically separates a first doped Silicon region from a second doped Silicon region.

7. The integrated circuit of claim 6, wherein the first doped Silicon region is exposed to a Silicon etch treatment.

8. The integrated circuit of claim 7, wherein the Silicon etch is used to pre-define a drill slot.

9. A fluid ejection device, comprising an integrated circuit including a shielding element.

10. The fluid ejection device of claim 9, wherein the integrated circuit is a multilayer integrated circuit comprising a drill slot through at least one doped

Silicon layer, the one doped Silicon layer, wherein the one doped Silicon layer is at least substantially divided by the shielding element into a first section enclosing the drill slot and a second section.

11. The fluid ejection device of claim 10, wherein the shielding element comprises a gate oxide layer disposed above a low conductance Silicon layer.

12. A print head, comprising a multi-layer integrated circuit, further comprising means for electrically isolating a sensitive section of a said circuit to prevent damaging side effects of a manufacturing process.

13. The print head of claim 12, further comprising a semiconducting die, a drill slot disposed throughout the die allowing the flow of ink, wherein said sensitive section comprises a region within a doped layer of the semiconducting die surrounding the drill slot.

14. A process of making a multi-layered integrated circuit, comprising the steps of:

forming, at the surface of a semiconductor die at least an insulating layer;

etching at least said insulating layer thereby forming a surface with both semiconductor areas and insulating areas;

doping said surface, such that said surface is formed from insulating areas and doped semiconductor areas;

wherein said surface comprises a doped semiconductor area separated from a second doped semiconductor area by an unbroken insulator area disposed above the semiconductor die.

15. The process of claim 14, wherein the step of forming at least an insulating layer on said first doped semiconducting layer comprises growing a gate oxide layer.

16. The process of claim 15, wherein the step of forming at least an insulating layer on said first doped semiconducting layer further comprises depositing a gate electrode layer.

17. The process of claim 16, further comprising depositing a Tantalum cavitation layer.

18. The process of claim 16, further comprising the step of treating said first doped semiconductor area with at least TMAH.

19. A process of manufacturing a multi-layered integrated circuit, comprising:

forming one or more conducting layers;

forming at least one shielding element isolating at least part of said one or more conducting layers;

further processing said one or more conducting layers.

20. The process of claim 19, wherein the step of forming at least one shielding element further comprises:

growing a gate oxide layer;

depositing a polycrystalline Silicon layer;

etching the gate oxide and polycrystalline Silicon layers using a mask; and

doping to increase exposed semiconductor conductance.

21. An ink jet print cartridge, comprising:

a print head, further comprising a multilayer integrated circuit comprising a shielding element and a drill slot through at least one doped semiconductor layer;

wherein the one doped semiconductor layer is at least substantially divided by the shielding element into a first section enclosing the drill slot and a second section.

22. A slot fed print head useful for ink jet printers, comprising:

a multi-layer integrated circuit, the circuit further comprising at least a Silicon die and a Tantalum cavitation layer;

a drill slot disposed through the Silicon die;

a doped Silicon region surrounding the drill slot at the surface of the Silicon die;

a gate oxide enclosure substantially enclosing the doped Silicon region surrounding the drill slot and disposed directly above low conductance Silicon die; and

a Polycrystalline Silicon layer disposed directly above the gate oxide enclosure, the Polycrystalline Silicon layer comprising a dissipating element connecting the Polycrystalline Silicon layer to ground;